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105. The integrated circuit of claim 104 where the planar layer contacts the lower end of the sidewall.

106. The integrated circuit of claim 104 where the planar layer has a graded stoichiometry.

107. The integrated circuit of claim 106 where the planar layer comprises multiple layers having mutually different stoichiometries.

REMARKS

Applicant has considered the Office Action mailed on April 24, 2002, and the references cited therewith. This amendment cancels claims 31-37, 39-47, and 55-70, and adds new claims 71-107. As a result, claims 48-54 and 71-107 are now pending in this Application.

The cited Chen patent, the Miyamoto patent, and the present invention all have the object of forming a silicided layer at the bottom of a contact hole in order to increase the conductivity of a wiring plug to be deposited in the hole. The cited patents achieve this with a deposition process which, as noted previously, creates problems with flatness of the layer and contamination. The invention achieves better results by resputtering conductive material which had already been sputtered—mostly at the top of the hole. This process difference also engenders a structural difference. Both Chen and Miyamoto require additional layers down the sidewalls of their contact holes, which, *inter alia*, detract from the diameter of a highly conductive metal wiring plug later added to the hole. Figs. 3A and 3B of the Application, in contrast, clearly show that the present contact holes have the conductive layers 354, 356 only at the bottom, and that the sidewalls consist entirely of the original insulator layer 312 that covers the substrate 310.

Newly added claims 71-107 reflect this facet of the invention.

Independent claim 71 recites beyond doubt a vertical side wall “consisting substantially entirely of the aforementioned layer of insulating material.” The sidewall has no other layers such as 5 and 7 of Miyamoto or 14, 14', 16, 16', 16A, 34, 34A, and 37 taught by Chen. Moreover, this aforementioned layer is the one that is earlier recited in claim 71 as “directly”

overlying the substrate. Only the layers 2 of Miyamoto and 13, 33 of Chen directly overlie the substrate—but these layers do not form the sidewalls of the contact hole. Accordingly, claim 71 distinguishes over the cited references individually or in any combination.

Claim 77 contains equivalent recitations, adding to claim 71 a recitation as to the increased flatness of the conductive layer.

Claim 82 follows claim 71, and further introduces a “graded stoichiometry” between the elements of the conductive layer. Applicant respectfully disagrees with the Office Action statement that col. 4 lines 7-12 of Chen show such grading “in the bottom layer,” as recited in the claim. The purpose of this passage is to set the stoichiometry of the layer so as to reduce depletion of the underlying junction area in the substrate during annealing. Chen’s conductive layer in the hole itself has only single stoichiometry.

Claim 87 defines the vertical wall as being “free of the conductive elements” of the earlier recited conductive material on the bottom. Miyamoto’s metal in layers 5 and 7 is just as thick in the sidewalls as it is in the bottom layer. Chen’s metal layers also appear in the sidewalls fully as in the bottom of the hole.

Claim 92 specifies this feature in terms that the sidewall is “substantially free of the metal” whose silicide forms the bottom layer.

Claim 97 covers an integrated circuit having one or more contact holes of the type described. A layer of insulating material overlies the substrate, and “only that layer” forms the sidewall of the contact hole. Again, both Miyamoto and Chen show only multiple layers on the sidewalls of their contact holes, suggesting neither purpose nor means for eliminating them.

The integrated circuit of claim 103 recites the metal silicide in the bottom layer, and then declares “the metal”—i.e., that metal forming a part of the bottom layer—is “substantially entirely confined” to the bottom surface. In Miyamoto and Chen, this metal extends all the way up the sidewalls.

The dependant claims incorporate all the features of their respective parents, and distinguish over the cited references in other ways as well. For example, claims 72-73, 88-89,

and 98-99 specify that while the bottom planar layer does contact the “lower end” of the sidewall, it does not “extend substantially up the sidewall from the bottom surface.” As before, Miyamoto and Chen have at least one layer on the bottom that extends all the way up the sidewall.

Claims 80-81 recite particular percentages for flatness of the planar bottom layer, “about 20% and “about 10%.” The passage of Miyamoto cited in the Office Action, col. 5 lines 3-4, merely asserts that the film has “uniform thickness,” without any quantization whatsoever. The Application states on page 12 lines 1-2 that what passes for “uniform” in conventional practice is 50% flatness. Flatness is always desirable; the question is how uniform is “uniform.” Any imputation of a specific number to Miyamoto is pure guesswork in the light of the present invention.

As another example, dependent claims 95 and 105 aver that the bottom planar layer has a “graded stoichiometry.” For the reasons given in connection with claim 82, the Chen reference does not in fact teach or suggest any gradation in stoichiometry of the planar or bottom layer, but concerns itself only with depletion of an active area in the substrate underneath the bottom layer. Claim 84 recites “multiple layers” having different stoichiometries, as shown in Fig. 3B of the Application. By no stretch of the imagination does Chen suggest this feature.

Applicant respectfully traverses the rejection of claims 48 and 50-54 under 35 U.S.C. §102 as anticipated by Chen. As noted above in connection with claim 82, the cited passage at col. 4 lines 7-12 of Chen show no such grading “in the bottom layer,” as recited in the claim. The purpose of this passage is to set the stoichiometry of the layer so as to reduce depletion of the underlying junction area in the substrate during annealing. The Application teaches a similar consideration, at page 15 lines 3-10, by way of showing how the present invention minimizes silicon depletion from the substrate. Therefore, Chen’s conductive layer in the hole itself has only single stoichiometry, and Chen cannot anticipate or even make obvious the invention recited in claim 48.

Dependent claims 50-55 incorporate all the recitations of their parent claim 48.

Claim 49 was rejected as unpatentable over Chen in view of Miyamoto under 35 U.S.C. §103. In the context of claim 49, the only element that Miyamoto brings to Chen is the aspect ratio of the hole. Therefore, no combination of Chen and Miyamoto reaches the

AMENDMENT & RESPONSE UNDER 37 C.F.R. § 1.116 - EXPEDITED PROCEDURE

Serial Number: 09/826,661

Filing Date: April 5, 2001

Title: LOW ANGLE, LOW ENERGY PHYSICAL VAPOR DEPOSITION OF ALLOYS

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language of a claim having both the stoichiometry recitations of parent claim 48 and the aspect ratio of daughter claim 49.

Conclusion

For the above and other reasons, Applicant respectfully urges that the claims now pending are in condition for allowance and requests reexamination under 35 U.S.C. 132. The Examiner is invited to telephone Applicant's attorney (612 373-6971) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Box AF, Commissioner of Patents, Washington, D.C. 20231, on this 19th day of August, 2002.

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